second gate insulating film, said second semiconductor layer comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said third impurity region is disposed so as to partially overlap with said second gate electrode, and

wherein a wiring is electrically connected to said third impurity region.

REMARKS

In the Final Rejection, the Examiner has a number of rejections. Each are traversed herein. Applicants will address each rejection in the order in which it appears in the Final Rejection.

I. §112 Rejection, First Paragraph

In the Final Rejection, the Examiner rejects Claims 3, 8, 16 and 21 under 35 USC §112 first paragraph as allegedly containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor at the time the application was filed had possession of the claimed invention. In particular, the Examiner states that the specification never discloses each of the first conductive layers of the n-channel TFT and the p-channel TFT comprises a single layer as claimed in claims 3, 8, 16 and 21.

Applicants respectfully submit that this feature is disclosed in the specification at page 17, lns. 11-12. Accordingly, it is requested that this rejection now be withdrawn.

OK

II. §112 Rejection, Second Paragraph

The Examiner also rejects Claims 1-26 under 35 USC §112, second paragraph, as being

indefinite. Each of these objections will be addressed below.

The Examiner states that in claims 1, 6, 14, and 19, it is unclear whether a portion of the second conductive layer partially overlaps the first impurity region and whether a portion of the second conductive layer partially overlaps the third impurity region. These objections are believed due to informalities in the language in the claims. Therefore, Applicants have amended the objected to portion of each of these claims as follows, which should overcome these objections:

not OK

> "wherein said first impurity region of said n-channel TFT is disposed so as to partially overlap[s] with a portion [which] of said second conductive layer which is in contact with said gate insulating film;"

and

> "wherein said third impurity region of said p-channel TFT is disposed so as to partially overlap[s] with [said] another portion [which] of said second conductive layer which is in contact with said gate insulating film."

The Examiner also states that in Claims 11 and 24[1], it is unclear whether the first gate electrode partially overlaps the first impurity region and whether the second gate electrode partially overlaps the third impurity region. Applicants respectfully submit that the language of each of these claims is very succinct on this point and that the there is no indefiniteness in the language therein. Accordingly, it is requested that these objections be withdrawn.

The Examiner also states that it is unclear in Claims 6 and 19 whether the second conductive layer does not overlap the second impurity region and whether "said second conductive film" should

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[1] The objected to portion of each of the claims recites:

"wherein said first impurity region is disposed so as to partially overlap with said first gate electrode" and

"wherein said third impurity region is disposed so as to partially overlap with said second gate electrode".

be "the second conductive layer." These objections are believed due to informalities in the language in the claims. Therefore, Applicants have amended these claims as follows which should overcome these objections:

> "wherein said second impurity region of said n-channel TFT is disposed so as not to overlap[s] with said second conductive [film] layer;"

Accordingly, it is respectfully submitted that the claims are no longer indefinite but are now in an allowable condition. Therefore, it is requested that this rejection now be withdrawn.

III. Prior Art Rejections

A. Rejection of Claims 11-13

The Examiner rejects Claims 11-13 under 35 USC §103 as being unpatentable over Miyasaka et al. This rejection is respectfully traversed.

Applicants have amended independent Claim 11 to recite that "wherein a wiring is electrically connected to said third impurity region". Hence, as clearly explained in the specification at page 20, lns. 8-12, the third impurity region in this claim is not a LDD region such as that shown in Miyasaka et al. but instead is a source or drain region. Therefore, Miyasaka et al. does not disclose or suggest the device of independent Claim 11, and Claim 11 and those claims dependent thereon are patentable over this reference.

B. Rejection of Claims 1-10

The Examiner further rejects Claims 1-10 under 35 USC §103 as being unpatentable over Miyasaka et al. in view of Chang et al. This rejection is respectfully traversed.

As the Examiner admits, Miyasaka et al. does not disclose or suggest a gate electrode having a first conductive layer and a second conductive layer, as recited in the claims of the present application. Therefore, the Examiner cites Chang et al.

However, independent Claims 1 and 6, as amended, recite that the "second conductive layer being in contact with...a top surface and side surfaces of said first conductive layer". This feature is clearly shown in Fig. 1 of the present application.

In contrast, Chang et al. only discloses the alleged second conductive layer 22a or 22b only in contact with the side surfaces of alleged first conductive layers 14a and 16a (see Fig. 5 of Chang et al.).

Hence, neither of the cited references disclose or suggest the device of amended independent Claims 1 and 6 of the present application. Accordingly, these independent claims and the claims dependent thereon are patentable over the cited references.

C. Rejection of Claims 14-23

The Examiner further rejects Claims 14-23 under 35 USC §103 as being unpatentable over Miyasaka et al. in view of Chang et al., further in view of Johnson.

As independent Claim 14 has been amended in a manner similar to that described above of Claims 1 and 6, this claim and the claims dependent thereon are also not disclosed or suggested by the cited references and should be allowed thereover.

D. Rejection of Claims 24-26

The Examiner further rejects Claims 24-26 under 35 USC §103 as being unpatentable over

Miyasaka et al. in view of Johnson.

As independent Claim 24 has been amended in a manner similar to that described above for Claim 11, this claim and the claims dependent thereon are also not disclosed or suggested by the cited references and should be allowed thereover.

E. Conclusion

Accordingly, for the above-stated reasons, the claims of the present application are patentable over the cited references and should be allowed.

Therefore, for at least the above-stated reason, the present application is in an allowable condition and should now be allowed. If any fee is due for this amendment, please charge our deposition account 50/1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

Dated: July 19, 2001

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Marked-up copy of the claims as amended:

Please amend the claims as follows:

1. (Twice Amended) A ferroelectric liquid crystal display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with [both said first conductive layer and] said gate insulating film and a top surface and side surfaces of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said first impurity region of said n-channel TFT is disposed so as to partially overlap[s] with a portion [which] of said second conductive layer which is in contact with said gate insulating film;

wherein said third impurity region of said p-channel TFT is disposed so as to partially overlap[s] with [said] another portion [which] of said second conductive layer which is in contact with said gate insulating film.

6. (Amended) A ferroelectric liquid crystal display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with [both said first conductive layer and] said gate insulating film and a top surface and side surfaces of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said first impurity region of said n-channel TFT is disposed so as to partially overlap[s] with a portion [which] of said second conductive layer which is in contact with said gate insulating film;

wherein said second impurity region of said n-channel TFT is disposed so as not to overlap[s] with said second conductive [film] layer;

wherein said third impurity region of said p-channel TFT is disposed so as to partially overlap[s] with [said] another portion [which] of said second conductive layer which is in contact with said gate insulating film.

11. (Amended) A ferroelectric liquid crystal display device having an n-channel TFT and a p-channel TFT over a substrate,

said n-channel TFT comprising:

a first gate electrode formed adjacent to a first semiconductor layer with a first gate

insulating film interposed therebetween, said first semiconductor layer comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region;

wherein said first impurity region is disposed so as to partially overlap[s] with said first gate electrode, and

said p-channel TFT comprising:

a second gate electrode formed adjacent to a second semiconductor layer with a second gate insulating film, said second semiconductor layer comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said third impurity region is disposed so as to partially overlap[s] with said second gate electrode[.], and

wherein a wiring is electrically connected to said third impurity region.

14. (Amended) A goggle type display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with [both said first conductive layer and] said gate insulating film and a top surface and side surfaces of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said first impurity region of said n-channel TFT is disposed so as to partially overlap[s] with a portion [which] of said second conductive layer which is in contact with said gate insulating film;

wherein said third impurity region of said p-channel TFT is disposed so as to partially overlap[s] with [said] another portion [which] of said second conductive layer which is in contact with said gate insulating film.

19. (Amended) A goggle type display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with [both said first conductive layer and] said gate insulating film and a top surface and side surfaces of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said first impurity region of said n-channel TFT is disposed so as to partially overlap[s] with a portion [which] of said second conductive layer which is in contact with said gate

insulating film;

wherein said second impurity region of said n-channel TFT is disposed so as not to overlap[s] with said second conductive [film] layer;

wherein said third impurity region of said p-channel TFT is disposed so as to partially overlap[s] with [said] another portion [which] of said second conductive layer which is in contact with said gate insulating film.

24. (Amended) A goggle type display device having an n-channel TFT and a p-channel TFT over a substrate,

said n-channel TFT comprising:

a first gate electrode formed adjacent to a first semiconductor layer with a first gate insulating film interposed therebetween, said first semiconductor layer comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region;

wherein said first impurity region is disposed so as to partially overlap[s] with said first gate electrode, and

said p-channel TFT comprising:

a second gate electrode formed adjacent to a second semiconductor layer with a second gate insulating film, said second semiconductor layer comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said third impurity region is disposed so as to partially overlap[s] with said second gate electrode[.], and

wherein a wiring is electrically connected to said third impurity region.